Acorn Video Specifications

A3000, A500/R200, A5000, A3010, A3020, A4000, A4

Acorn Video Specification

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Introduction

This document outlines the Video systems implemented on the following current Acorn machines.

• A3000	9 w PGA
• A500/R200	9 w PGA
• A3010/A3020/A4000	15w VGA (enhanced)
• A5000	15w VGA (enhanced)
• A4 portable	15w VGA (enhanced) built in LCD display

It is assumed that the reader is familiar with the basic concepts of computer systems built around the ARM micro-processor unit (MPU) and its associated support devices, MEMC, VIDC and IOC. Some background information on VIDC implementation is detailed in VIDC overview.

In this document logic low active signals are indicated by a backslash / before the signal name,

Detailed specifications on the ARM chip set can be found in the Prentice Hall publication:

Acorn RISC Machine Family Data
Book ISBN 0-13-781618-9.

VIDC Overview.

The Video controller uses three buffers in RAM to generate three functions, a video display, a hardware cursor and stereo sound. The memory controller (MEMC) coordinates the transfers from these buffers to VIDC by Direct Memory Access (DMA). The Video controller requests data from memory when required, and stores it in one of three internal "first-in, first-out" (FIFO) buffers. Data is requested in blocks of four 32-bit wide words, allowing efficient use of page-mode DRAM without slowing down the system data bus for long periods.

The data from these buffers is serialised via digital to analogue converters (DACs). Video data is checked with a colour look-up palette, before being converted to analogue signals, red, green and blue (RGB) for video monitors. The use of DACs allows minimal external buffering for audio systems or video monitors.

Three forms of video synchronisation pulses are generated with programmable timing and polarity. The video clock may be selected from a variety of sources, and appears on external pins to allow the video to be genlocked to an external source.

The video controller is programmable offering a variety of display formats. The pixel rate can be selected from a range of sources and programmable pre-scaling applied. Video data be serialised to 8,4,2 or 1 bits per pixel. The horizontal timing parameters can be controlled to units of two pixels, and the vertical timing is controlled to units of one raster.

The 13 bit colour look-up palette to the DACs allows a choice from 4096 colours, or an external video source.

The hardware cursor is 32 pixels wide and may be any number of rasters high. It can be positioned anywhere on the screen. Three simultaneous colours(from a palette of 4096) are supported, and any pixel can be defined as transparent, which makes it possible to define cursors of varied shape.

The sound system on VIDC incorporates an exponential DAC and stereo image table for generation of high quality sound. Up to 8 channels are supported, each with a separate stereo position.

Video Interface Descriptions.

A3000 System Summary

The A3000 uses a standard combination of ARM2 CPU and MEMC + data bus controlling VIDC.

A3000 Connectors and Links

The A3000 has a 9 way D-type RGB video socket. This has a standard IBM PC PGA pin layout (SK14)

1	Red
2	Green
3	Blue
4	Horizontal or Composite Sync (Link 24)
5	V.Sync or Mode (Link 25)
6,7,8,9	0V

RGB video levels are 0.7V PK-Pk into 75 Ohm
Sync Voltage levels >= 2.0V (TTL) into 75 Ohm

An asterisk * indicates default

Link 24	Link pins 1,2 for H.Sync
	Link pins 2,3 for C.Sync *
Link 25	Link pins for V.Sync
	No link for Mode
(A3000 International)	
(Link 25	Link pins 1,2 for V.Sync)
	Link pins 2,3 for Mode *)
Link 26	Linked H.Sync inverted
	No link H.Sync standard *
Link 27	Linked V.Sync inverted
	No link V.Sync standard

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The A3000 has a Monochrome Video Output Phono socket (SK 13) providing a monochrome composite video signal of 1V Pk-Pk (0.7V video and 0.3V sync) into a 75 ohm load. Negative sync, positive video.

Link pins within the machine are provided to facilitate connection to a Genlock interface.

Link 28	pin 1	Ckvidc	
	pin 2	/Clksys	
Link 29	pin 1	0 V	
	pin 2	Sink	
Link 30	pin 1	/V.Sync or C.Sync	
	pin 2	/H.Sync	
Link 31	pin 1	/Supremacy	(On issue 1)
	pin 2	0 V	(On issue 1)

Genlock Signal Descriptions:

Ckvidc: VIDC master clock input. (TTL). VIDC resynchronises all it's inputs to this reference allowing the display frequency to be independent of processor and system tinting.

/Clksys: 24MHz sytem clock. CMOS, buffered signal supplying MEMC with a master clock reference used to derive all system timing functions. This is often used to supply Ckvidc, with a shorting link on Link 28.

Sink: External synchronisation pulse, TTL level input. A high on this signal resets the vertical timing counter and if an interlaced signal display is being used, the odd field is selected. The horizontal timing counter and all other registers are unaffected by this signal.

/V.Sync or C.Sync CMOS level output. Depending on bit seven of the Control Register, *this* pin will be either /V.Sync or C.Sync. V.Sync pulse width supplied by VIDC is programmable in units of a raster and if selected is active low. The C.Sync signal is the XNOR of /V.Sync and /H.Sync

/H.Sync This is a CMOS level output required by some monitors. It is also used by MEMC to discriminate between Cursor and Video requests. The pulse is active low, and the pulse width supplied by VIDC is programmable in units of 2 pixels.

/SUP: Supremacy CMOS level output signal. The signal can control a multiplexer between VIDC outputs and an external source for video mixing. If bit 12 of the Video or Cursor palette for any logical colour is set /SUP is driven low when that logical colour is displayed. So any logical colour can be defined as supreme or not, on a pixel by pixek basis.

A3000 Video Output Circuit.

Each Video output signal from VIDC is a current sink with respect to the filtered video +5V supply. The signals (Red, Green and Blue) generate a voltage across a sense resistor and a PNP transistor.
The voltage across the sense circuit is converted to an output current per colour, by a PNP transistor emitter follower. Another set of three PNP transistors are used in common mode to sum the three signals which are then added to /Composite Sync to provide the Composite Monochrome video out on SKT 13. The RGB monitor output components and Monochrome output components are protected from transients by a three diode circuit for each colour signal. A 220R load resistor limits the maximum unterminated voltage at each transistor collector; this ensures the transistor does not saturate and disturb the sense resistor signal. In normal use the RGB outputs generate an analogue 0.7V peak signal into an external 75R load to GND.
Separate or composite sync signals can be generated within VIDC under software control When selected, the Composite Sync signal appears on the V.Sync line. Sync signal outputs use a Cmos driver with a 68R resistor in series. The sync output can drive a monitor with TTL level inputs, typical of VGA and multi-frequency monitors, or an analogue 75R terminated sync input.

A540/R260 System Summary

A540/R260 systems use a combination of ARM 3 (on a daughter card) with MEMC, databus and Video clock MUX to control VIDC.

A540/R260 Connectors and Links

These machines have a 9 way D-type RGB video socket with a standard IBM PC PGA pin layout (SKT 2)
This is an identical pinout to that described for the A3000 (SKT 14) as are the RGB and Sync voltage levels. An additional link is provided to allow Sync on Green

SKT 12 High resolution mono video output. Provides a 0.7V mono video signal into 75 Ohm at a dot rate of 96 MHz. This requires a high resolution monitor to be connected.

SKT 13 High res mono Vertical/Composite Sync.

SKT 14 High res mono Horizontal Sync.

Link 1 Internal auxiliary video connector (molex pins) providing access to the following signals:

1 Red
2 Green or Sync on Green (Link 2)
3 Blue
4 Horizontal or Composite Sync (Link 6)
5 V.Sync or Mode (Link 3)
6 0 V

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An asterisk * indicates default

Link 2 Link pins 1,2 for Sync on green
Link pins 2,3 for normal Sync *

Link 3 Link pins 1,2 for V.Sync to ROB D-type pin 5
Link pins 2,3 for Mode to pin 5 *

Link 6 Link pins 1,2 for H.Sync to RGB D-type pin 4
Link pins 2,3 for CSync to pin 4 *

A Video control latch (&3350048) is used by the operating system to control clock speed and video sync polarity appearing at SKT2, SK13/14 and Link 1. These data bits are latched and provide the following:

DB0	0	DB1	0	24 MHz
DB0	0	DB1	1	25.175 MHz
DB0	1	DB1	0	36 MHz
DB0	1	DB1	I	Reserved

				V.Sync	H.Sync
DB2	0	DB3	0	+ve	+ve
DB2	0	DB3	1	+ve	-ve
DB2	1	DB3	0	-ve	+ve
DB2	1	DB3	1	-ve	-ve

Link 15 Genlock expansion I/F. This is two 2 rows of 8 Molex pins, numbered as shown below. As a default, shorting links connect pins 1-2, and 3-4.

	Pins		
Intck	1	2	Ckvidc
Sink	3	4	OV
NC	5	6	NC
/Ved 0	7	8	/Ved 1
/Ved 2	9	10	/Ved 3
/Supremacy	11	12	/Hi
/H.Sync	13	14	/V.Sync or C.S
0 V	15	16	0V

Genlock Signal Descriptions
(See other Genlock Signal descriptions for A3000)

Intck: The clock output from a programmable clock signal multiplexer, enabled by the video latch allowing the clock frequencies shown above.

/Ved 0-3: Video external data outputs (CMOS) levels. The inverse of the four data bits fed to the red DAC are output on these pins. With an external serialiser a very high resolution monochrome display may be obtained, and is the basis of the high res monochrome output on SK13 for these machines.

/HI: Horizontal I/F timing marker (CMOS o/p). With interlaced displays this signal goes low halfway along the raster, staying low until the end of the raster. If non-interlaced displays are used then this signal may be used for a programmable timer on each raster

A540/R260 Video Output Circuit

Differences from A3000:
The sync signal polarity is programmable and there is the additional facility to put Sync on the Green output.

The Monochrome video output uses video external data Ved[0-3] which is serialised using a shift register running at 96 MHz providing a high resolution Monochrome output.

A5000 System Summary

The A5000 machine uses ARM 3 in combination with MEMC and databus, with IOEB supplying CLK to control VIDC.

A5000 Connectors and Links

The A5000 machine has a 15 way mini D-type RGB video socket. (SK1)

1	Red
2	Green
3	Blue
4	ID 2
5,6,7,8	0 V
9	+5V (750 mA fuse)
10	0V
11	ID 0
12	ID 1 or SCART function
13	Horizontal Sync
14	V.Sync or Composite Sync
15	ID 3

The A5000 has no other external Video connector. Internal link pins are provided within the machine to facilitate connection to a Genlock Interface.

Link 6 Genlock interface.
This is identical to the Genlock I/F pin layout of the A540 series shown above. (Link 15) The signal descriptions are the same.

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A5000 Video Output Circuit

Differences from A3000:

The RGB signals generate a voltage across a sense resistor and a common super-diode, formed by a PNP transistor, ie the current sense for each channel is handled by one transistor instead of three. This means they are no longer completely isolated from each other and each colour will have a very slight effect (considered negligible)on the other colours.

There is no monochrome output, or sync on green.

A5000 RGB Enhancements:

The pin layout of SK2 is very similar to a standard VGA pinout, but with several enhancements, detailed below:

- Pin 9 (normally, used for keying) is used to supply +5v specifically for powering an external UHF modulator. The output is protected by a 750mA fuse.
- Pin 12 provides +12V (source impedance = 1k5). This output is used to provide a SCART function switching signal for use with SCART TVs.
- Pin 15 is an input ID 3 which may be used in the future to identify standard monitor types.

A5000 Monitor Types

The monitor types listed below are supported. A scheme of automatically sensing the monitor type connected to the computer is implemented. This scheme ensures that the user sees a picture regardless of whatever monitor type is connected to the computer and that, where possible, the complete list of modes available for the particular monitor type is made available.

	Monitor Type	Modes
0:	TV frequency/SCART TV/UHF modulator	0-17,24,33-36
1:	Multi-frequency monitor	0-21,24-31,33-46
3:	VGA monitor	0-15,25-28,41-46
4:	VGA/Super VGA mon	0-15,25-31,41-46

The automatic sense scheme uses the four ID bit inputs (ID0-3) present on the video interface connector to detect die type of monitor connected to the computer. The ID bits are read directly by software, where data bits D0-D3 correspond to ID0-ID3. Monitors designed for use with IBM machines and compatibles use a coding system where these bits define the monitor type. The bits are either connected to 0V or are left open circuit in the monitor or monitor cable. All ID bits are connected to 4K7 pullups on the A5000 PCB.

For example a mono VGA monitor connects ID1 to 0V leaving ID0 and ID2 to float high. This ID system has been adopted and extended as shown in the table:

Monitor Type	ID Settings ID3	ID2	ID1	ID0
Mono VGA	*	1	0	1
Colour VGA	*	1	1	0
Colour SVGA	*	0	1	0
Multi-frequency (using comp sync)	*	H.Sync	1	1
TV/UHF mod SCART	*	1	1	HSync

* undefined

Note 1: If none of the ID bits are connected to 0V then the software will default to the TV frequency monitor.

Note 2: The H.Sync to ID bit connections are Acorn defined and are made in the monitor cable.

A5000Monitor Sensing

The *Configure options: Monitortype, Sync and Wimpmode have an AUTO setting (eg. *Configure Monitortype Auto) which determines the operation of the automatic monitor type sensing scheme.
At power-on or following a hard reset, with all three options set to AUTO, the software senses the monitor type and sets the Wimpmode, Sync type and Monitor type (which defines the list of available modes) for the particular monitor connected. These are temporary values which are not written back to the CMOS RAM. Subsequent *Configure Monitortype, Sync or Wimpmodes selected by the user overwrite the relevant AUTO setting in CMOS RAM so the machine is initialised in the mode desired. A new power-on/reset sequence is the same as described above, except that software now uses the options selected by the user instead of the AUTO setting. See the figure Monitor Sensing on the following page.

Most Multi-frequency monitors have their ID bits set as if they were a VGA or Super VGA monitor, and monitor type 1 modes will be available when using the monitor sensing scheme, as many Multi-frequency monitors are capable of displaying some or all of the monitor type 1 modes. To use genuine SVGA monitors re-configure the CMOS RAM setting to monitor type 4.

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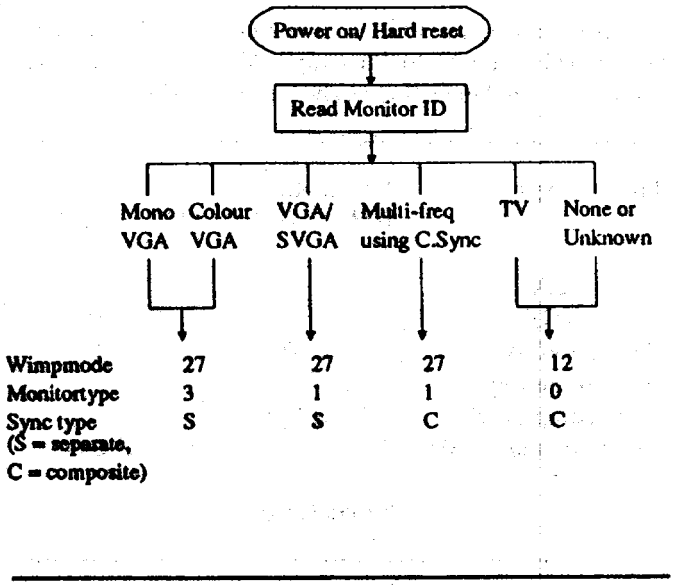

A3010/A3020/A400₀ System Summary

These systems use the ARM250 combination chip. This contains an ARM 2AS processor, MEMC. IOC and VIDC all within a single chip, and so the overall system architecture is fundamentally the same.

A3010/A3020/A4000 Connectors & links

These systems have a 15 way mini D-type RGB video socket (SK1) with the same pin layout and specification as that described for the A5000, including the enhanced monitor sense protocol.

A Genlock interface is provided, signal pins as follows.

Link 6	PINS		
/H.Sync	1	2	/V. or /C.Sync
sink	3	4	0V
Vidclk	5	6	Clkvid
0V	7	8	/Sup

The signal descriptions are identical to those described for the A3000.

A3010/A3020/A4000 Video Output Cct

Differences from A3000:

A3010, A3020 and A4000 are identical to A5000.
A3010 also has a pair of emitter followers for each colour. One set is for RGB monitor signals, and the other is for the TV colour encoder circuit detailed below.

Separate or composite sync signals can be generated within the ARM 250; selection is software controlled. When selected, the Composite Sync signal appears on the V.Sync line. Sync signals are CMOS buffered.

A3010 TV Colour Encoder

The RGB current sources driving the colour encoder each generate a a nominal 0.7V peak signal across a terminating 75R resistor. The RGB signals are capacitively coupled to the encoder Ic inputs. A Sony CXA1145 encodes the RGB video and TTL. composite sync signal into a colour video signal (ie; Video + composite sync + chroma (colour) signal).
The chroma signal can be set to PAL or NTSC formats. For PAL 1 (UK), a 4.4336 MHz crystal is used in the CXA1145 oscillator circuit. .A trimmer capacitor allows the fine tuning of the carrier frequency. In practice the frequency is not critical for colour generation in a TV but the chroma frequency does beat/interfere with high frequency components in the luma signal. Careful trimming of the oscillator can reduce the subjective effects of the beat frequency.
The chrona signal is band-pass filtered before it is mixed with the delayed luma signal. The luma delay is chosen to match the chroma signal delay through the bandpass filter. the complete encoded signal is terminated with a two-resistor attenuator, which matches the signal level to the UHF modulator. A separate bias chain ensures the correct DC level is present at the rnodulator input. The modulator is a standard video plus sound unit which generates a low power UHF signal -on channel 35 (UK model).

A4 System Summary

The system uses ARM3 in conjunction with MEMC and databus to control VIDC. For the LCD display there is a controller ASIC (LC ASIC), which also controls VIDC clock signal.

A4 RGB Connector

This machine is fitted with a 15 way mini-din Video RGB connector (SK6). The pin out is identical to A5000 and Monitor types are sensed using ID bits in the same way.

A4 also supports monitor type 5 which is the LCD screen option. If nothing is connected to SK6 then the machine assumes the LCD is required. A summary. of Monitor types supported by A4 machines are shown below.

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	Monitor Type	Modes
0:	TV frequency/SCART TV/UHF modulator	0-17,24,33-36
1:	Multi-frequency monitor	0-21,24-31,33-46
3:	VGA monitor	0-15,25-28,41-46
4:	VGA/Super VGA mon	0-15,25-31,41-46
5:	LCD screen	0-17,24-28
AUTO	Auto-configure	Monitor dependent

There is no Genlock I/F, or monochrome output. There are no links for video functions.

A4 Video Output Circuit

Differences from A3000:

The RGB output circuit is identical to that described for the A5000. The only slight mechanical difference is that the RGB signals from VIDC go to a video hybrid board, which contains the common super diode current sense circuitry, protection diodes and transistor drivers, before returning to the main PCB for connection to SK6.

A4 LC ASIC Description

The LC asic provides a programmable interface to monochrome flat panel LCD displays offering 16 levels of grey scale. A large range of display formats are catered for including 320X200 and 640X200 single panel displays as well as 640X400 and 640X480 dual panel displays.
The device accepts pixel data, and horizontal and vertical sync signals from VIDC. It re-times the image and converts it to grey scales for display on the LCD panel.

When used to control a dual panel display, one or two external DRAMS are needed to act as a half frame buffer. The LC ASIC supports a wide variety of DRAMs, though in most applications, two 64Kx4 devices are sufficient.

A4 LC ASIC Functions

The following functional blocks are contained within the LC ASIC.

CLOCK: Clock and reset inputs used with LC's crystal oscillator provide clock selection and control for LC and VIDC.

VIDC l/F: The VIDC interface block synchronises incoming video data and sync signal, and inverts incoming data before performing a logical to physical colour translation. It does this by looking up the logical colour on the 16 entry on-chip palette.

REGISTERS: This functional block contains all the software programmable bits in the device and outputs them to other parts of the chip via the Control logic block.

CONTROL: This generates all the internal control logic signals.

GREY SCALE: The grey scale block takes input from the VIDC interface post-palette data and control block to provide Grey scale video data to the DRAM block.

DRAM: This block takes data input from the Grey scale block, together with Control and Clock signals, in order to store data temporarily in the external DRAM devices, generating all necessary timing and control signals for them. The DRAM block also outputs the data to the LCD panel; with the correct timing.

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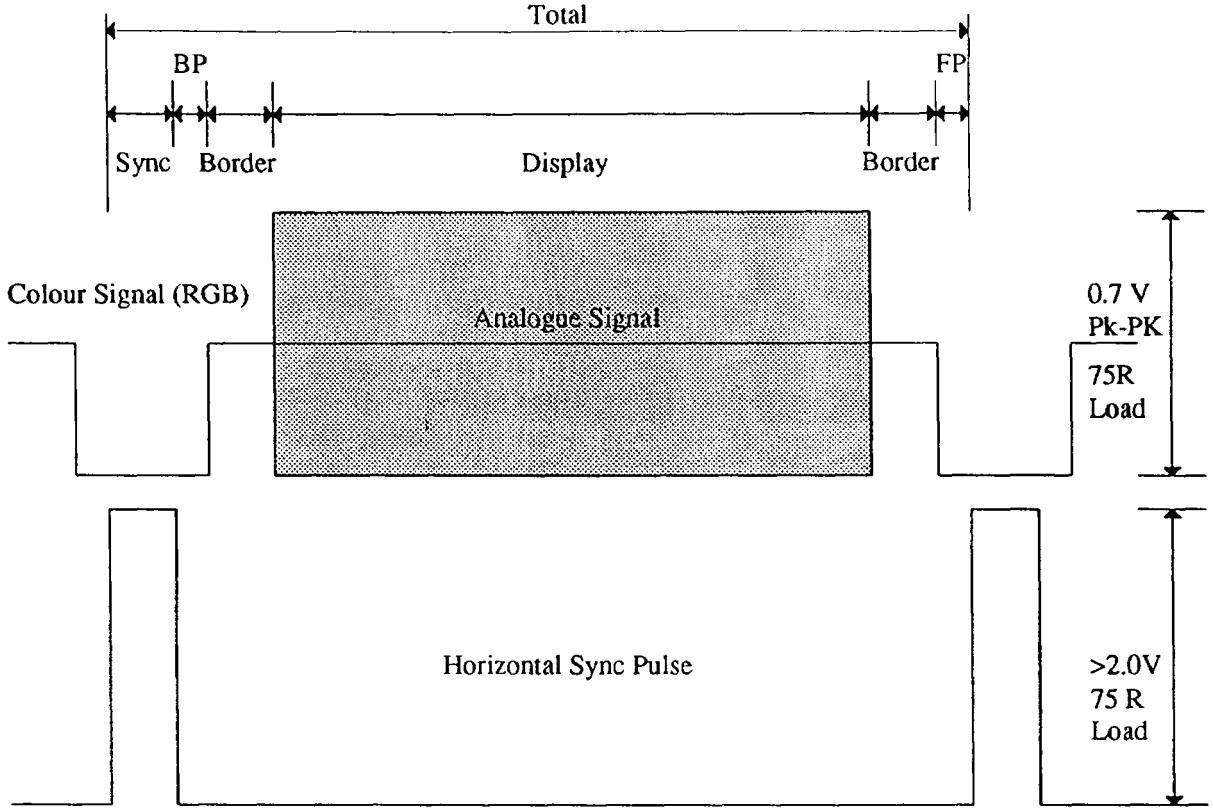
RGB Key Diagram



Monitor Type 0 Horizontal Parameters

Mode	Sync	Back Porch	Border	Display	Border	Front Porch	Total		H.freq KHz	Display Center uS	Pixel Rate KHz
0,3,4,8,11	76	89	96	640	96	27	1024	pixels	15.625	36.31	16000
12,14,15	4.75	5.56	6.00	40.00	6.00	1.69	64.00	uSec			
1,2,5,6,7	38	45	48	320	48	13	512	pixels	15.625	36.37	24000
9,10,13	4.75	5.62	6.00	40.00	6.00	1.62	64.00	uSec			
16,17,24	114	133	96	1056	96	41	1536	pixels	15.625	36.29	16000
	4.75	5.54	4.00	44.00	4.00	1.71	64.00	uSec			
33,35,35,36	76	121	0	768	0	59	1024	pixels	15.625	36.31	16000
(overscan)	4.75	7.56	0	48.00	0	3.69	64.00	uSec			
TV nominal	76	90	0	832	0	26	1024	pixels		36.40	16000
	4.75	5.65	0	52.00	0	1.60	64.00	uSec			

Monitor Type 0

Note; Raster values in brackets apply for Risc OS 2 instead of Risc OS 3.

Vertical Parameters

									H.freq Hz	Vertical Center
0,1,2,4,5,8,9										
10,12,13,15	3	19(20)	16	256	16(15)	2	312	rasters	50.08	166
3,6,7,11,14,17	3	19(20)	19	250	19(18)	2	312	rasters	50.08	166
33,34,35,36	3	19	0	288	0	2	312	rasters	50.08	166

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Monitor Type 1 — Horizontal Parameters

Mode	Sync	Back Porch	Border	Display	Border	Front Porch	Total		H.freq KHz	Display Center uS	Pixel Rate KHz
0,3,4,8,11	72	63	88	640	88	73	1024	pixels	15.625	33.94	16000
12,14,15	4.5	3.94	5.5	40.00	5.5	4.56	64.00	uSec			
1,2,5,6,7	36	31	44	320	44	37	512	pixels	15.625	33.87	8000
9,10,13	4.5	3.87	5.5	40.00	5.5	4.62	64.00	uSec			
16,17,24	108	73	106	1056	106	87	1536	pixels	15.625	33.96	24000
	4.5	3.04	4.42	44.00	4.42	3.62	64.00	uSec			
33,35,35,36	76	83	0	768	0	97	1024	pixels	15.625	36.94	16000
(overscan)	4.75	5.19	0	48.00	0	6.06	64.00	uSec			
18,19,20,21	56	113	0	640	0	87	896	pixels	26.786	20.37	24000
	2.33	4.71	0	26.67	0	3.62	37.33	uSec			
25,26,27,28	96	47	0	640	0	17	800	pixels	31.469	18.39	25175
(VGA)	3.81	1.87	0	25	42 0	0.68	31.78	uSec			
29,30,31	100	101	0	800	0	23	1024	pixels	35.156	16.69	36000
(SVGA)	2.78	2.81	0	22.22	0	0.64	28.44	uSec			
37,38,39,40	118	59	0	896	0	27	1100	pixels	21.818	26.04	24000
(DTP-ega)	4.92	2.46	0	37.33	0	1.12	45.83	uSec			
41,42,43	76	37	0	640	0	15	768	pixels	21.853	25.8	16783
(EGA-pcemu)	4.53	2.2	0	38.13	0	0.89	45.76	uSec			
44,45,46	72	163	0	640	0	145	1020	pixels	15.686	34.69	16000
(CGA-pcemu)	4.5	10.19	0	40.0	0	9.06	63.75	uSec			

Monitor Type 1 — Vertical Parameters

0,1,2,4,5,8,9 10,12,13,15 16,24	3	16	17	256	17	3	312	rasters	H.freq Hz 50.08	Vertical Center 164
3,6,7,11,14,17	3	16	20	250	20	2	312	rasters	50.08	164
33,34,35,36	3	19	0	288	0	2	312	rasters	50.08	164
18,19,20,21	3	18	0	512	0	1	534	rasters	50.16	277
25,26,27,28	2	32	0	480	0	11	525	rasters	59.94	274
29,30,31	2	22	0	600	0	1	625	rasters	56.25	324
37,38,39,40	3	9	0	352	0	0	364	rasters	59.94	188
41,42,43	3	9	0	352	0	0	364	rasters	60.04	188
44,45,46	3	34	0	200	0	25	262	rasters	59.87	137

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Monitor Type 2 Horizontal Parameters

Mode	Sync	Back Porch	Border	Display	Border	Front Porch	Total		H.freq KHz	Display Center uS	Pixel Rate KHz
23	52	47	2	288	2	1	392	pixels	15.625	33.94	24000
Hi res Mono	2.17	1.95	0.08	12.0	0.08	0.04	16.33	uSec			

Monitor Type 2 Vertical Parameters

23	3	43	4	896	4	0	950	rasters

Monitor Type 3 Horizontal Parameters

Mode.	Sync	Back Porch	Border	Display	Border	Front Porch	Total		H.freq KHz	Display Center uS	Pixel Rate KHz
0,3,4,8,11	96	47	0	640	0	17	800	pixels	31.469	18.39	25175
12,14,15	3.81	1.87	0	25.42	0	0.68	31.78	uSec			
1,2,5,6,7,9	48	23	0	320	0	9	400	pixels	31.469	18.35	12587
10,13	3.81	1.83	0	25.42	0	0.71	31.78	uSec			
VGA nominal	96	40	0	656	0	8	800	pixels	31.466	18.43	25175
12,14,15	3.81	1.59	0	26.06	0	0.32	31.78	uSec			

Monitor Type 3

Vertical Parameters

								H.freq Hz	Vertical Center
10,12,13,15 16,24	2	106	0	256	0	85	449	rasters	70.09	236
3,6,7,11,14,17	2	109	0	250	0	88	449	rasters	70.09	236
VGA 350, nom	2	53	0	362	0	32	449	rasters	70.08	236

Monitor type 4 (VGA/SVGA)

Monitor type 4 parameters are the same as all monitor type three modes, plus Monitor type 1 parameters for modes 25, 26,27,28 (VGA) and 29,30,31 (SVGA)

Monitor Type 5 (LCD) Horizontal Parameters

Mode	Sync	Back Porch	Border	Display	Border	Front Porch	Total		H.freq KHz	Display Center uS	Pixel Rate KHz
0,3,4,8,11	108	175	0	640	0	269	1192	pixels	20.134	25.12	24000
12,14,15 25,26,27,28 41,42,43,44 45,46	4.5	7.29	0	26.67	0	11.21	49.67	uSec			
1,2,5,6,7,9	54	87	0	320	0	135	596	pixels	20.134	25.08	12000
10,13	4.5	7.25	0	26.67	0	11.25	49.67	uSec			

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Monitor Type 5 (LCD) Vertical Parameters

Mode	Sync	Back Porch	Border	Display	Border	Front Porch	Total		H.freq Hz	Vertical Center
10,12,13,15	1	0	112	256	116	0	485	rasters	41.51	241
3,6,7,11,14	1	0	115	250	119	0	485	rasters	41.51	241
25,26,27,28	1	0	0	480	4	0	485	rasters	41.51	241
41,42,43	1	0	64	352	68	0	485	rasters	41.51	241
44,45,46	1	0	140	200	144	0	485	rasters	41.51	241